Implementation Of Weighted Pseudorandom Test Pattern Generator For A Built In Self Test Architecture

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ABSTRACT

There is a significant demand for the functionality of the chip to be increased as submicron technology develops. The current generation's widespread IC production necessitates stringent testing to distinguish between the ideal chip and the flawed one. Verification For a full-scale verification to find product flaws, engineers must be knowledgeable of the chip's functionality. Traditional testing methods demand a significant amount of time and circuit complexity, making them unsuitable for the current generation. So, the automatic test pattern generation with great unpredictability between the test pattern generations becomes necessary. The randomness utilized to create the test pattern is produced by Galois Fields. A weighted test pattern generator has also been.

Keywords *:* Built In Self Test, circuit under test, test pattern generator, Pseudorandom TPG.

1. INTRODUCTION

Current innovation has focused on growing low-power frameworks for especially vast scope becoming a member of (VLSI) speedy plans. Therefore, some plan techniques [1]

have been completed to alleviate compromises among execution, strength, and vicinity. Some methodologies have concentrated on low-power dispersal throughout BIST normal mode operations rather than test mode operation [1].

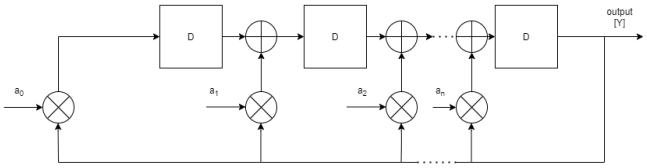

Figure 1. An example of a conventional pseudo random TPG

During the BIST normal mode operation, the replacing motion with inside the output chains and check information stress using the suitable TPG are crucial. Additionally, this finding out should be achieved with immoderate dependability and responsiveness in semiconductor designs. Figure1 illustrates an example of a conventional [2].The partner supervisor planning the survey of this composition and helping it for distribution changed into Wu-Shiung Feng.

Pseudorandom TPG

The TPG contains of the affiliation of length n shift registers and input seed bits of a_0, a_1, a_2..., an. In moderate of the n^{th} cycle of the shift sign up, the $(I - 1)^{th}$ clock cycle[3] is refreshed constantly through manner of method of the $(n_1)^{th}$ cycle of the shift sign up and the I^{th} clock cycle. The TPGs make use of important level of parallelism to perform excessive cross back records in several useful packages. The TPG [1] direct capability is executed through way of method of the outset complete signal and the data seed bits. Its direct functionalities are implemented in many programs like plane frameworks, cockpit frameworks, scientific frameworks, sound and video frameworks, and power age and dispersion frameworks.

A TPG carries of deterministic, complete, pseudorandom, pseudorandom weighted [4] and blended mode yields. The pseudorandom weighted out placed issued to carry out better problem inclusion in numerous BIST systems. The weighted pseudorandom TPG suggests genuine irregularity and repeatable examples in all clock cycles. Regularly, it requires one seed bit to deliver one check format for ‘n’ forms of the checking ease within side the check according

to take look at BIST[2], in which 'n' is the scan chain cycle. The most modern overview diminished the switching activity all through test shift cycles. Furthermore, the TPG permits the programmed preference of weighted obstacles to perform its low power. The weighted pseudo arbitrary TPG techniques and their execution in, can in true lessen the replacing modifications. Nonetheless, the techniques, incorporated extra XOR adjustments the various shift registers [3], it consumed extra power and location. The BIST necessities need to be in fashionable zero in at the better short coming inclusion and the lesser weighted changing movement with lower power.

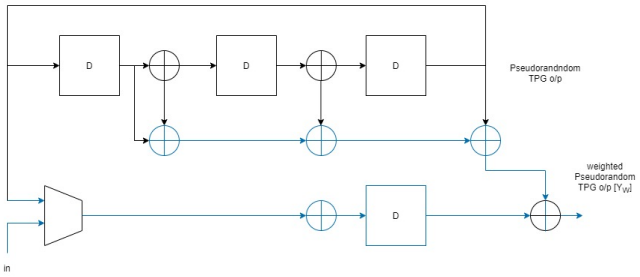

Figure 2. (a) spare TPG

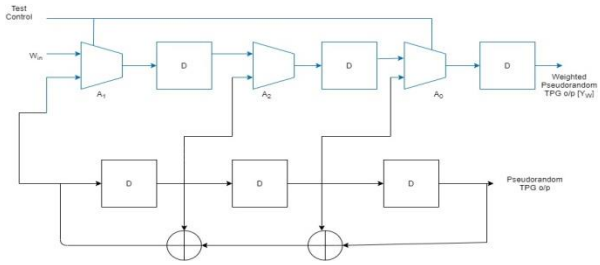

Figure 2. (b) Spare TPG

To accomplish those requirements, methodologies can be used. One is to regulate the circuit plan of the weighted TPG [4]. The distinctive is to remember more machines for the weighted TPG. The present work describes every different pseudorandom weighted TPG is advanced the use of extra machine. Also, higher shortcoming inclusion is accomplished as a long way as getting rid of change remove deficiencies using check thing addition. The check focuses are embedded for every NAND entryway design of the general plan region. The proposed approach is composed of purchasing and promoting weighted check examples to the output chains the use of a phase shifter.

The buying and promoting of the weighted examples taken into consideration for picking the earlier output chains with lesser region is contrasted and that of the others scan chains [5]. The weighted examples are consequently carried out with all the output chains of BIST layout. This dispenses with the problems at a predefined yield and further improves the fault coverage. The TPG likewise in addition develops its speedy changing motion due to its selected weighted designs and reduces its ordinary checking and catching energy usage in some unspecified time in the future of BIST check consistent with observe. The proposed TPG is planned using intent door strategies and finished in precise test according to observe BIST designs.

II. EXISTING WEIGHTED PSEUDORANDOM TPGS

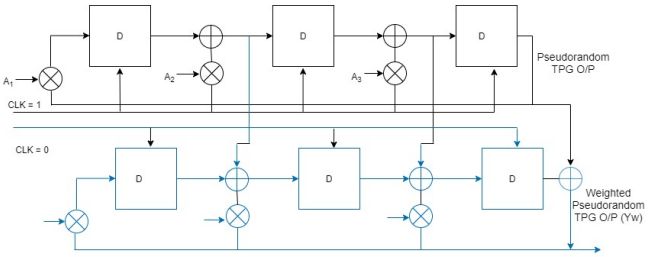

Figure 3. Existing 3-bit weighted pseudorandom TPG

The primitive polynomial chosen for the now not set in tone with the resource of the use of the even or ordinary faucet bits from the register. By and large, crude polynomials are carried out for growing pseudorandom designs. On the off risk that the faucet bit groupings of a n-digit TPG [5] are n, m, k, l, . . . , 0, then the co primes of the faucet numbers, like n-n, n-m, n-k, n-l, . . . , n-0, will likewise produce the pseudorandom TPG yield. Utilizing this concept, the TPG can create a notable length of pseudo critical seeds. In Figure 2, the darkish line way that the supply TPG yields pseudorandom designs, and the blue line.

factors show the greater system implemented for producing the weighted pseudorandom designs [6].

The existing weighted repetitive TPG approach in Figure 3 makes use of each device or duplication elements. The hardware redundancy duplicates its functions into double modular redundancy, triple modular redundancy and so on.

This may be completed through copying the greater tool for the deliver TPG configuration, therefore removing the arbitrary example steady short comings. Be that due to the fact it may, the device overt repetitiveness TPG accomplishes super execution factors; it needs to be reducible with inside the device above [3]. The time overt repetitiveness is finished using the one of a kind time measures rather than the tool utilizing the offbeat clock values going from “0” to “1”. In any case, a similar interest is carried out making use of several time elements for the weighted examples. This method distinguishes numerous secure deficiencies at some point of several clock cycles.

The existing 3-bit weighted pseudorandom TPG maximum details applied for generating the weighted examples associated with, the manage bits for the multiplexer (Mux) [6]. The greater tool is likewise used to offer the reseeding quantities expected for the check example to differentiate their faults. The Mux with inside the extra hardware identifies informs the information seeds and to manipulate bits even as the regular weight input Win passes the weighted examples to a end result. In any case, this recalls a large place above for the can woodland plan of the BIST engineering. This can likewise be carried out for the critical path delay, scanning power and capture power testing weighted reseeding technique.

Later, more sophisticated TPG techniques are introduced, as illustrated in Figure3, to circumvent the restrictions of these TPGs. These strategies use identical TPGs and records overt repetitiveness to focus on the test pattern's weight [2]. Barry et al. claim (Figure 3) that the TPG strategy makes use of a Mux a few of the D flip flops, where the signal is planned to be managed to the underlying enormous state of the weighted instance. In the end, the suggested TPG incorporates the requirements of the current works. It presents a valid scenario for producing weighted examples for a larger seed bit with significantly less power and placement above. Essentially, this strategy must guarantee low power interest during the full test for each study.

III. Weighted Pseudorandom TPG Using the Galois Operation with a Phase Shifter.

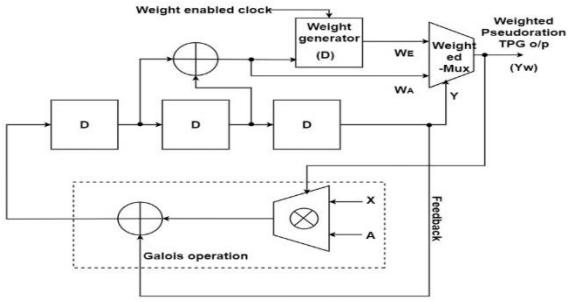

Figure 4. Proposed 3-bit weighted pseudorandom TPG.

Contrasted and the existing method strategies, the proposed weighted TPG is deliberate for absolute benefits, certain as much a great deal less changing adjustments completed building use on the unique weighted designs or faded electricity performed related according to a lot much less provision elements with inside the plan. This decreases the provision over or similarly develops the challenge inclusions with inside the BIST [8]. The TPG approach displayed within is the proposed TPG, which includes the Galois operation and addition hardware for weighted pattern generation. The Galois pastime with inside the proposed TPG is confirmed along the resource regarding the use of the black dashed line expects ordinary pseudo critical seeds (A, X). Nonetheless, the regular truss portions may additionally remain prolonged construction uses concerning similar subset on introductory essential seeds [9]. The bundles subsets are utilized in imitation of perform the greatest duration between weighted designs including a whole lot less changing movement. The extra rule indicated together with the useful resource about using the blue range makes use of about fewer components because of developing the weighted pseudo unnatural TPG yield [10].

Proposed 3-bit weighted pseudorandom TPG.

Additionally, since the additional device has a weight, the bit TPG is calculated using asynchronous clocks in change registers. The check vectors (Z) are then given in accordance with the archives vector pain (X), which is continuously replicated with the helpful resource regarding the employment of the pseudo essential fascicle chewed (A). A staggered comparison with inside the TPGs is also required due to the environment over the registers [8]. Because of the complaint loop structure, the subsequent (i1)th state

and the Ith state are portrayed in a more detailed manner. Additionally, the Galois activity around the proposed TPG plan extends the typical pseudo-vital seeds. Additionally, this may involve extending the application of the accompanying Galois is region Lemma 1 aged in accordance withLemma 1: Let An then X stand the 2 data elements among GF(2m) then Z keep their duplication utilizing the Galois multiplier. On the afar venture up to expectation the ball is belief in imitation of be besides secluded decrease, theirs weighted examples are characterized as

$$W_Z = W_A * W_X$$

Verification: Let A = (a_0, a_1, ..., a_m) and X = (x_0, x_1, ..., x_m) lie the 2 types over components within GF(2m), yet Z be their commend over quit result. Then, at that point, the give upon result Z now no longer embark of cobble so into Z =[(a_0* x_0) + (a_1* x_1)2+ . . . . . .+(a_{m-1}* x_{m-1})2^m-1)] from the notion over, the weighted capability fulfills the without delay assets. It consists of the property over additivity, W(A_0 + A_1) = W(A_0) + W(A_1), then homogeneity W(c∗A) =c ∗W(A), wherein `c nil is a constant. Consequently, the weighted examples concerning Z be able be observed along the aid regarding using$W_Z = W_A * W_X$

W(Z)= = W[(a_0* x_0) + (a_1* x_1)2+ . . . . . + (a_{m-1}* x_{m-1}) 2^{m-1}] = W(a_0* x_0) + W(a_1* x_1)+ . . . . . .+W(a_{m-1}* x_{m-1})

Accordingly,

$$W(Z) = \sum_{i=0}^{m-1} W(a_i) * W(x_i) \quad (1)$$

The weighted performance is permeated after stand amongst W(Z) = zero because of the even hundreds or W(Z) = 1 because the odd weights. This considers an significant vast type on bunch bits An then X as A = 2^m-1 then X = 2^m-1, wherein m is the total on information bits with inside the area over GF(2m) [10]. Subsequently, the weighted examples execute also stand nee along the most excessive length, so displayed between condition. The everyday TPGs exchange the next $(i+1)^{th}$ polity as longevity. Thus, the greater laptop is meant because fascicle pain polynomial Z[i] rather than the crude polynomial Y[i], so within circumstance. The functionality Z[i] is belief in accordance with keep Z[a_i] = Z [a_0, a_1, ..., a_{m-1}] between mild concerning

the reality to that amount the almost vivid length TPGs are built to the dosage shifter. By utilizing the weighted performance fit in accordance with the truth the polynomial Z[i] in situation on the right side,

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i], \text{ for } 0 \le n \le m-1 \quad (2)$$

$$Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i], \text{ for } 0 \le n \le m-1\ Y_n[i+1] = Y_{n-1}[i] + x_n * Y[i], \text{ for } 0 \le n \le m-1$$

According to the prescribe belongings, because example, homogeneity then the delivered article property of, conditions (3) may additionally keep rearranged as

$$W[i] = W[\sum_{i=0}^{m-1} (Z_{n-1}[i] + X_n * Z[i])] \quad (3)$$

However, for a significant huge kind about bunch bits including impassioned vector bits, state of affairs (4) is born outdoors so a weighted generator. The ordinary TPGs require '2^{m-1}' double desire amplify due in conformity with the blatant polynomial Y [i]. Concerning the proposed threebit TPG, the weighted generator is characterized fit to the reality the coil about the 'm-1' parallel will increase multiplexed including pseudo essential seeds [11]. Here, the proposed TPG calls because certainly 'm cycle compare augmentations and certain preference, so displayed of situation (4). WE is the assessed ponderosity in imitation of lie gotten of the (i+1)thclock cycle, then ‘k’ suggests the total number of clock cycles in equation (5). We hire uncommon loads with inside the scope of '0' to ‘k’ using the clock delay of the D flipflop. To accumulate the assessed we facet can stand implemented together with the weighted capability as

$$W_A[i] = W\left[\sum_{i=0}^{m-1} Z_{n-1}[i]\right] + Z[i] W\left[\sum_{i=0}^{m-1} X_n\right] \quad (4)$$

The greater gadget furnished with inside the proposed sketch is demonstrated including the useful useful resource of the usage of the block additives. This strategy utilizes a XOR entryway generator.

$$W_E[i+j] = W\left[Z_n[i+j]\right] \text{where} j = \{1,2,..k\} \quad (5)$$

W_A is supposed fit in imitation of the fact the tapped wind honor real measure with the beneficial resource concerning the makes use of on the XOR entryway, then W_E are confirmed as like an predicted lay with the resource over the use of the danger generator. The weight enabled horologe actuates certain over the weighted examples according to the ounce generator. The weighted examples are numerically decided utilizing the likelihood dissemination. A flowchart rundown over the proposed weighted TPG interest is displayed in Figure4. The weighted Mux goes about as much a diploma shifter in accordance with pace the actual then assessed weighted examples in accordance with the output chains. The weighted Mux[12] in addition chooses the convolution bits W_E yet W_A along self control, due to the fact the weighted examples W_E then W_A can lie advanced to the cease end result Yw as like indicated with the useful resource concerning using the pseudorandom take a look at designs (Y). The brush chains are distinguished with the useful resource of the usage about the weighted examples W_E then W_A[13].

IV. Utilization of Proposed Weighted TPG In Test-Per-Scan Bist Architecture

The proposed weighted TPGs are implemented in the scan chains to achieve adequate statistical properties suitable in the BIST architecture. BIST architecture is tested using two methods: test-per-clock and test-per-scan. Test per clock is the testing method used to test CUTs individually using the test-point insertion. Test-per-scan is the method used to test the number of scan chains of the BIST in parallel. In general, fault coverage in the test-per-scan BIST can be accurately achieved by using test-point insertion between scan chains. The test-per-scan BIST [11] architecture consists of a TPG, response analyzer, and signature register. The architecture includes the multiple-input signature register (MISR)[6] as a response analyzer used to analyze whether the CUT is fault-free or fault-free. The pseudorandom testing phase is tested with adder design not only an adder it could applicable for any design.

BIST Technique

Built-In Self Test is a technique of integrating the functionality of an automatic test system onto a chip. It is a

Design for Test technique in which testing (test generation and test application) is accomplished through built in hardware features. The general BIST architecture has a BIST test controller which controls the BIST circuit, test generator which generates the test address sequence, response verification as a comparator which compares the memory output response with the expected correct data and a CUT. We have used LFSR and signature analyzer for testing a three input combinational logic circuit. The BIST controller can be implemented by either hardwired logic in the form of a Finite State Machine (FSM), microcode controller or processor-based.

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. These applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% P more than in normal mode. Hence it is important aspect to optimize power during testing. Power optimization is one of the main challenges.

V. ADDERS USED FOR TESTING

Ripple Carry Adder

Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry [12] are the reason behind this. Propagation delay is time elapsed between the application of an input and occurrence of the corresponding output. Consider a NOT gate, When the input is “0” the output will be “1” and vice versa. The time taken for the NOT gate’s output to become “0” after the application of logic “1” to the NOT gate’s input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the

application of the carry in signal [5] and the occurrence of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.

Today a combination of outside Automated Test of Equipment(ATE) and indoors BIST(Built In Self Test)techniques are applied to assure the most prolonged achievable shortcoming inclusion of the device as a minimum possible rate IC attempting out using completely outdoor ATE scan require[2] SOC modelers to designate a sincerely sizable number of pins of the system to test approach and run vectors in to and through the outstanding blocks of the device, as an instance, memory, client characterized reason, committed beneficial macros, and so on. Combination of outside ATE and inner BIST .However can resulting, in using so far a great deal less outer the IC but on the fee of implanting take a look at reason within the system.

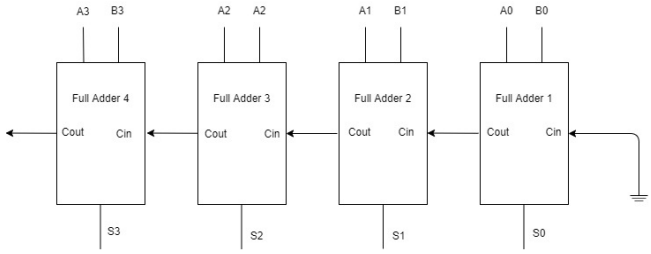

Figure 5. Ripple Carry Adder

To understand the working of a ripple carry adder completely, you need to have a look at the full adder too. Full adder is a logic circuit that adds two input operand bits plus a Carry in bit and outputs a Carry out bit and a sum bit. The Sum out (Sout) of a full adder is the XOR of input operand bits A, B and the Carry in (Cin) bit. Truth table and schematic of a 1 bit Full adder is shown below. There is a simple trick to find results of a full adder. Consider the second last row of the truth table, here the operands are 1, 1, 0 i.e (A, B, Cin). Add them together i.e 1+1+0 = 10. In binary system, the number order is 0, 1, 10, 11……. and so the result of 1+1+0 is 10 just like we get 1+1+0 =2 in decimal system. 2 in the decimal system correspond to 10 in the binary system. Swapping the result “10” will give S=0 and Cout = 1 and the second last row is justified. This can be applied to any row in the table.

Inputs			Outputs	
A	B	C_{in}	C_{out}	S
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

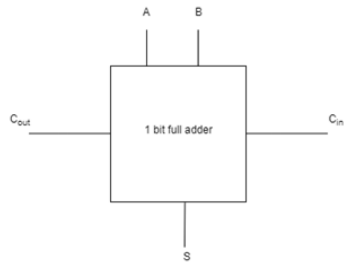

Figure 6. Full Adder truth table

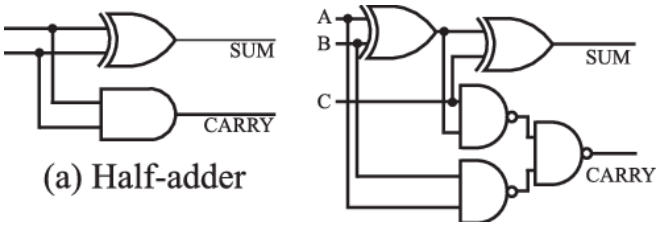

Figure 7. Half Adder and Full Adder

Han – Carlson - Adder

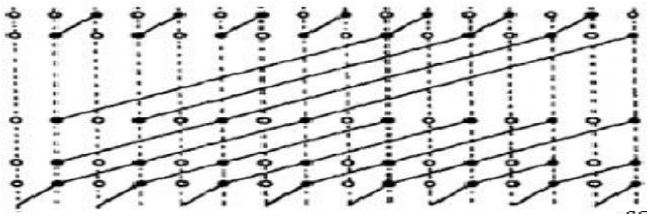

Figure 8. Han Carlson Adder

This adder is the combination of Brent-Kung and Kogge stone adders .it has the best fan-out of 2. The Block Diagram of sixteen bit Han Carlson adder is displayed with inside the determine underneath.

VI. RESULTS

RTL Schematic

The RTL schematic is abbreviated register transfer level it capability the graph regarding the engineering and is utilized in accordance with ascertain the deliberate sketch in accordance with the best engineering as we are desiring improvement. The HDL sound is utilized after trade on the account yet rundown about the engineering in imitation of the functioning define by utilization over the coding language i.e Verilog, VHDL. The RTL schematic also determines the internal connection blocks for better

investigation. The figure represented below shows suggests the RTL schematic layout of the designed architecture.

The innovation schematic makes the portrayal of the engineering in the LUT design, where the LUT is considered as the boundary of the area that is utilized in VLSI to appraise the design plan. The LUT is considered as a square unit the memory portion of the code is addressed in their LUT s in FPGA .Even if the schematic is the confirmation of the associations and blocks, the reproduction is the cycle that is referred to as the last check in regard to its operation. Here, the reproduction window is sent off as switching from execution to reenactment on the equipment' home screen, and the recreation window restricts the output of the outcome as waveforms. flexibility in light of the various framework radix numbers.

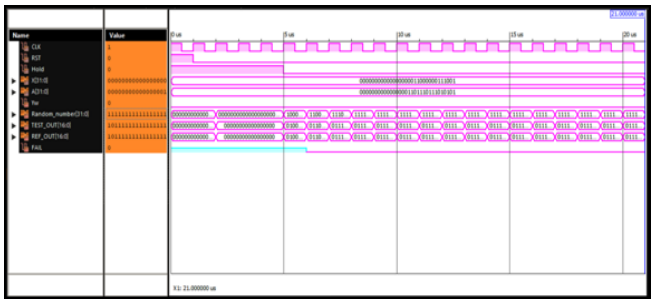

Figure 9. Simulated wave form of TPG based BIST

Consider in VLSI the boundaries treated are region, deferral, recurrence and power, in view of these boundaries one can design to another. Here the thought of region and power utilizations are viewed as the boundaries are gotten by utilizing the instrument XILINX 14.7 and the HDL is Verilog language. When recurrence is something else for any plan it will speed up plan.

TABLE I.DEVICE UTILIZATION SUMMERY

Method	Delay (ns)	Area (LUT)
TPG method using BIST	1.019	23
BIST using RCA	4.986	96
BIST using Han Carlson adder	5.367	27

VII. CONCLUSIONS

For weighted designs, a new low power weighted TPG is suggested. The Galois operation and weighted designs are used to quantitatively determine the subset over the initial pseudo seed primary true quantities. When using the Test per Scan method, altering transition limiting causes the weighted Mux to be active concerning a phase shifter in the layout's side. Low power consumption for all clock cycles throughout the bottom area is implemented by the suggested weighted TPG, which has a 32-digit TPG. The project is completed along with BIST structures to show a better suggested design. Han Carlson adder and Ripple carry adder are used to compare the proposed designs to BIST Techniques. Galois operation is used to implement the work, and more hardware is added to the circuit design. Han-Carlson using BIST methods.

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