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Design And Implementation Of High Speed Low Power Mux Based Full Adder Using 16nm Technology

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ABSTRACT

In this Project, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. We also propose six new hybrid 1-bit full-adder (FA) circuits based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, powerdelay product (PDP), driving ability, and so on. To investigate the performance of the proposed designs, extensive HSPICE and Cadence Virtuoso simulations are performed. The simulation results, based on Tanner the 16-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other FA designs. A new transistor sizing method is presented to optimize the PDP of the circuits. In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for optimum PDP with less iteration. The proposed circuits are investigated in terms of variations

of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors

I.INTRODUCTION

In today's world, now day's electronic systems plays a crucial role in day to day life. Digital Gadgets e.g., microprocessors, communication devices, and signal processors, are part of electronic systems. As the demand for electronic systems increases, the usage of circuits [1] are restricted to consume low power and area consumption. Therefore, as there is growth in population and technology the demand for the portable devices such as mobile phones, tablets, and laptops have increased a lot , so the designers to meet the above requirement ,designs the circuit which consumes low energy consumption and area with the increase of speed. As the efficiency of many digital applications are to perform arithmetic operations, such as adder circuits, multipliers circuits and dividers schematics. As the technology is developed the chip density for the design of circuit is increased. So the plenty of transistors are doped into the single chip.

II.EXISITNGMETHOD

The Existing method XOR–XNOR circuit is saving almost 16.2%–85.8% in PDP, and it is 9%–83.2% faster than the other circuits. The circuits of Fig. 1(d) and (e) have the very high delay due to its output feedback (which have the slow response problem). As can be seen in Table I, the efficiency of Fig. 1(e) is much worse and its delay is four times more than that of other circuits. Table I indicates that the structures have shown a better performance, which have the minimum NOT gates on the critical path and also have not feedback on the outputs to correct the output voltage level. To better evaluate the XOR–XNOR circuits, they are simulated at different power supply voltages from 0.6 to 1.5 V and also at different output loads from FO1 to FO16. The results of these two simulations are shown in Fig. 5(b) and (c). As seen in Fig. 5(b) and (c), the proposed XOR–XNOR circuit has the best performance in both simulations when compared with other structures.

The two input signal A, B are given to transistors. The signal B is given to P2 and signal A is given to P3.The signal B is given to N2 and P4 and the signal a is given to N2 and N3.The N3 is connected to P4.The signal B is given to N4 and P6 and the. Signal A is given to P5 and P6

The N4 is connected to N5.The signal B is given to N5 and the signal A is given to N6.The transistors P4 and N4 are shorted together and the out is A_{bar}. The signal A is given to N9 and C_i is given to P9.The N2 and N3 transistors are shorted together and output is given N7 and C_i is given to N7, C_i is given to P7.the N2 and N3 transistors are shorted together and output is given N7 and N8. The P5 and P6 transistors are shorted together and output is given P7 and P8 C_i is given to N8, P8. The output to N2 and N3 is given to N9 and P9 and output of P5 and P6 is given to N10 and P10.The signal C_i and B is given to N10 and P10.The output of N7 and P7 and output of N8 and P8 are shorted together and the output is sum. The output of N9,P9 and N10,P10 are sorted together and output is carry. The circuit is simulated in 65nm technology and result are obtained.

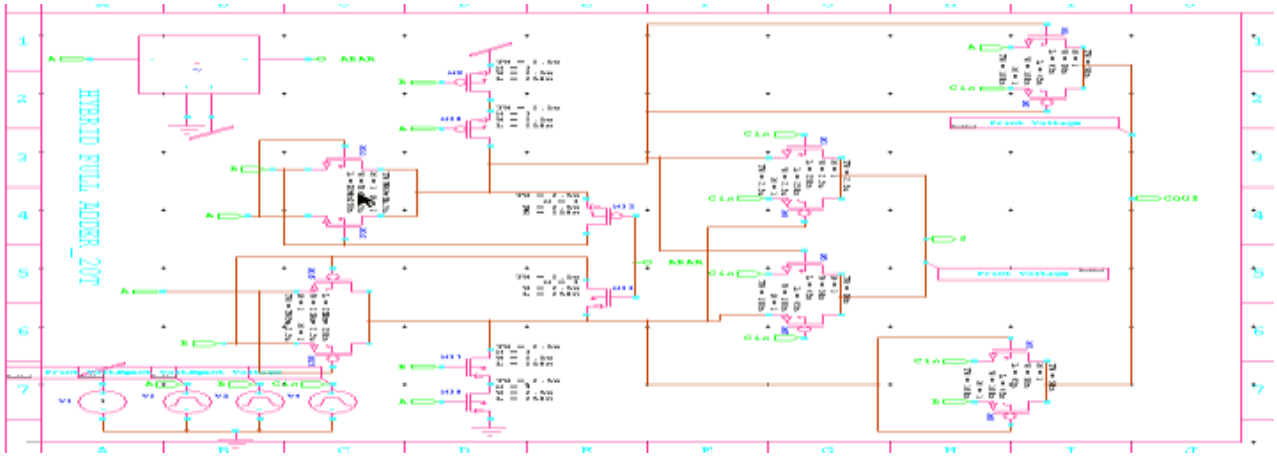


FIG :2.1 Schematic Of Hybrid Full Adder-20 Transistor

The above figure shows the schematic of hybrid full adder - 20 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

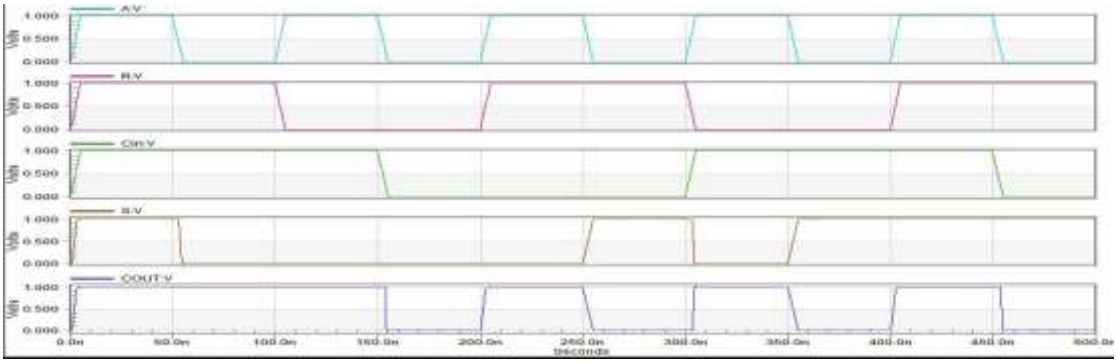


FIG 2.2: Simulation Of Hybrid Full Adder-20 Transistor

the above figure shows the PDP analysis of Hybrid Full Adder-20 Transistor. It analyzed by using tanner tool. The PDP is 340.98.For above simulation have done with 0.8 VDD.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is $A_{bar.}$The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to p8 and n8.The signal C_i is given P9 and N9.

The signal C_{ibar} is given N10 and P10.The signal C_{ibar} is given N11 and P11.The output of N9,P9 and N10,P10 are shorted together and is given to inverter which consist of P12 and N12 ,the output of inverter is sum. The output of N8,P8 and N11,P11 are shorted together and is given to inverter which consist of N13 and P13 ,the output inverter is carry**.** The circuit is simulated in 65nm technology and result are obtained.

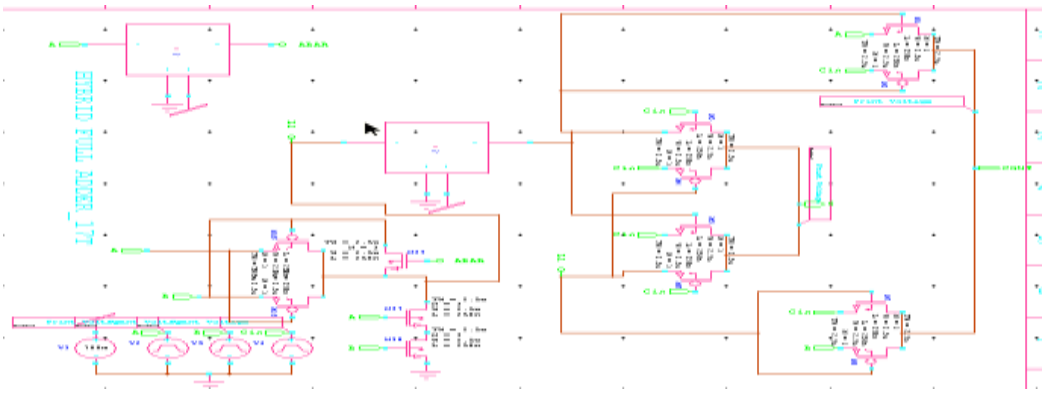


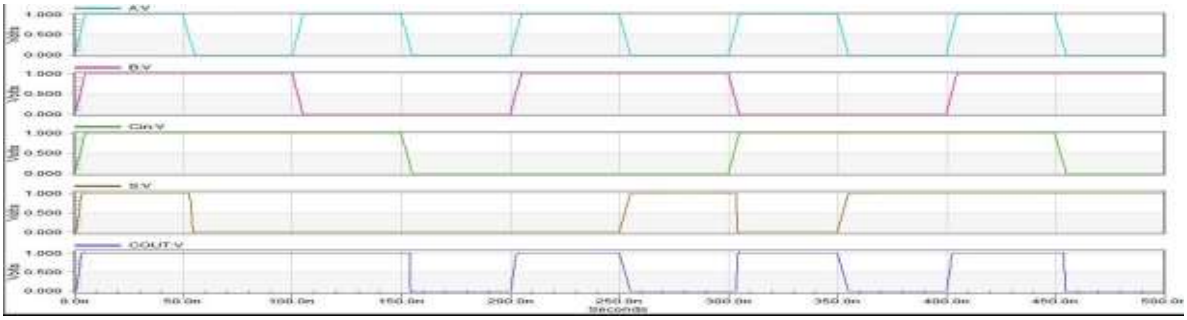
FIG 2.3: Simulation of Hybrid Full Adder-17 Transistor

The above figure shows the schematic of hybrid full adder 17 T transistors which is combinations of number of PMOS and NMOS logic is designed in 16 nm technology .It is designed with tanner S-EDIT Tool.

FIG 2.4: Simulation of Hybrid Full Adder17 T Transistor

The above figure shows the simulation results of Hybrid Full Adder17 T Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The above figure shows the PDP analysis of Hybrid Full Adder17 T Transistor. It analyzed by using tanner tool. The PDP is 291.1505 .For above simulation have done with 5 VDD.



The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A

is connected to N7.The output of P5 and N5 is A_{bar} .The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to inverter which consist of P12 and N12.

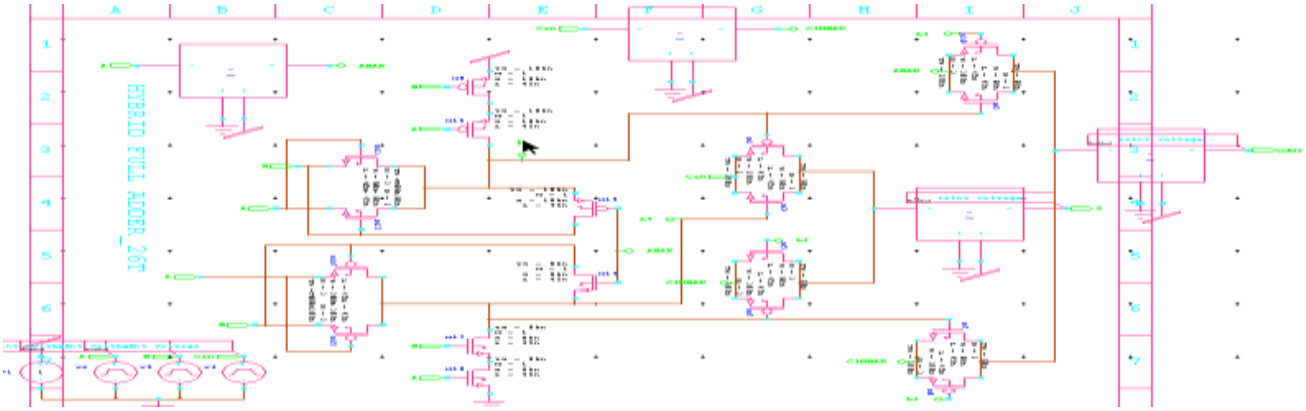


FIG 2.5: Schematic Of Hybrid Full Adder -B-26Transistor

The above figure shows the schematic of hybrid full adder -B-26 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool. The above figure shows the simulation results of Hybrid Full Adder-B-26Transistor.It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is $A_{bar.}$The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to inverter which consist of P12 and N12.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 [2]and the signal

A is connected to N7.The output of P5 and N5 is $A_{bar.}$The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to p8 and n8.The signal C_i is given P9 and N9.

The signal C_{ibar} is given N10 and P10.The signal C_{ibar} is given N11 and P11.The output of N9,P9 and N10,P10 are shorted together and is given to inverter which consist of P12 and N12 ,the output of inverter is sum. The output of N8,P8 and N11,P11 are shorted together and is given to inverter which consist of N13 and P13 ,the output inverter is carry**.** The circuit is simulated in

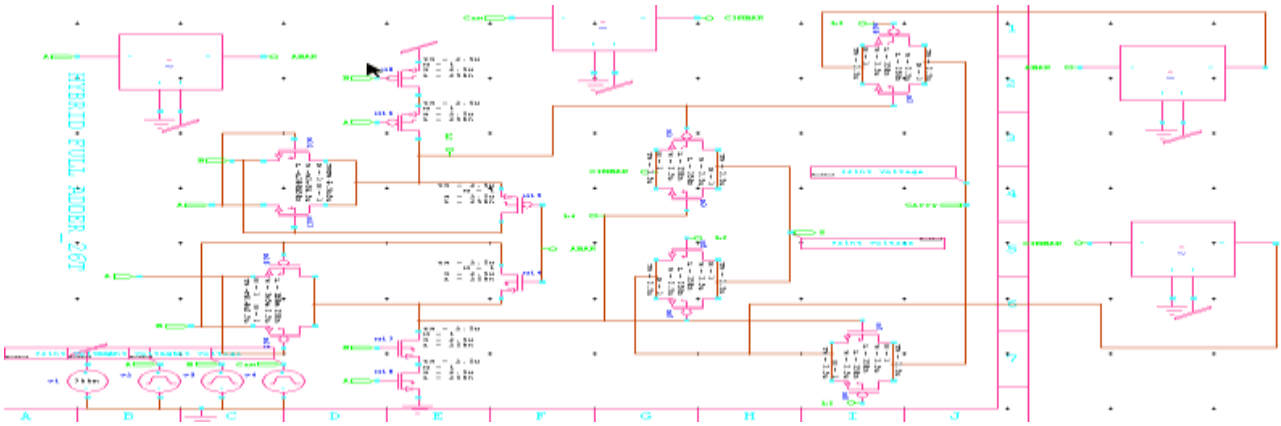
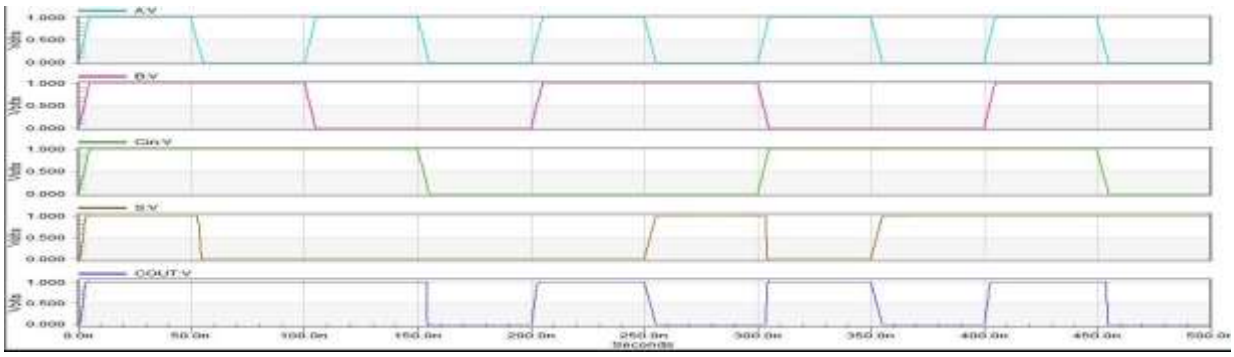
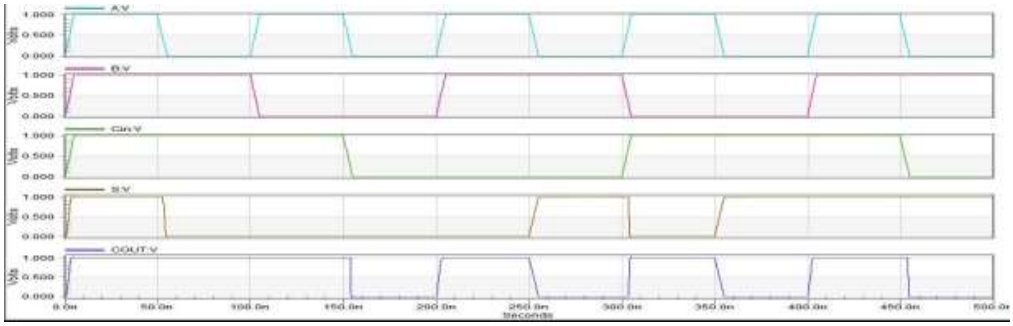


FIG 2.6: Schematic of Hybrid Full Adder HFA-NB-26T.



The above figure shows the schematic of hybrid full adder - B-26 transistors [3]which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool

FIG 2.7: Simulation of Hybrid Full Adder-B-26 Transistor.



The above figure shows the simulation results of Hybrid Full Adder-B-26Transistor.It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor). The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 .The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7.The output of P5 and N5 is $A_{bar.}$The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal A_{bar} is given to inverter which consist of P12 and N12.

The signal A,B are given to P4,P3.The transistor P4 is connected P5.The signal B is given to N3 and P5.The signal A is given to N3 and N4.The signal A is given to P6 and P7 [4].The signal B is given P7 and N5.The transistor N5 is connected N6.The signal B is connected N6 and the signal A is connected to N7. The output of P5 and N5 is $A_{bar.}$ The output of N3 and N4 is given N8 , P9,N10 and P11.The output of P6 and P7 is given to P10,N11,P8 and N9.The signal B is given to P8.The signal A is given to N8 .The signal $C_{i\ bar}$ is given P9 and N9.The

Signal C_i is given N10 and P10.The signal C_i is given N11 and P11.The output of N9,P9 and N10,P10 are shorted together and the output is sum. The output of N8, P8.

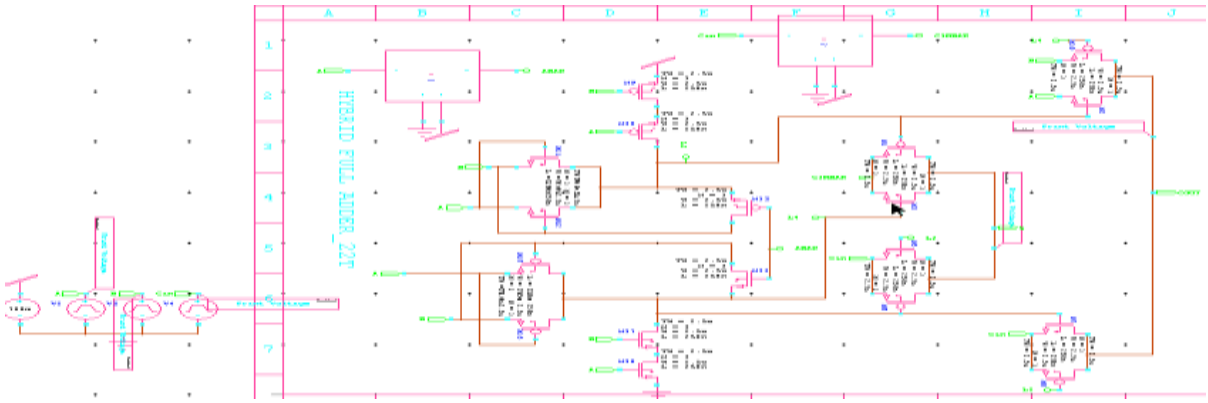


FIG 2.8: Simulation of Hybrid Full Adder HFA- 22T

The above figure shows the schematic of hybrid full adder - 22 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

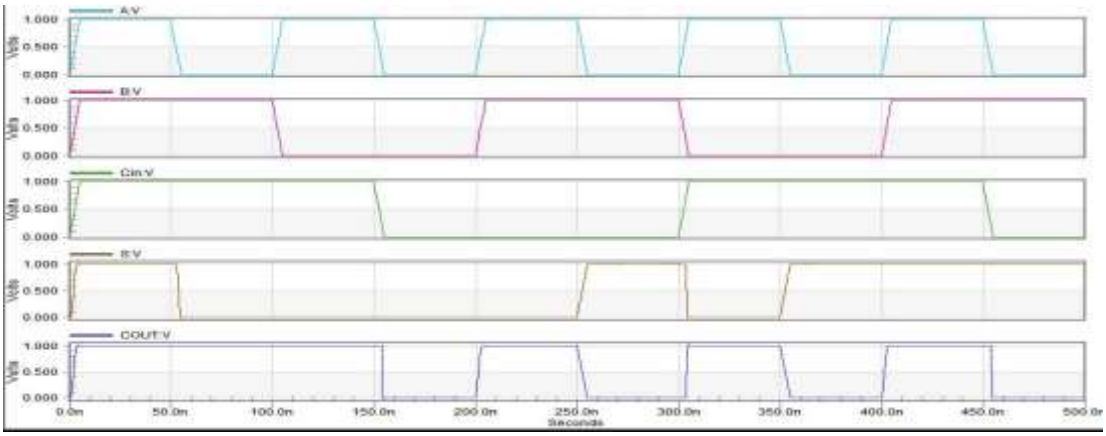


FIG 2.9 Simulation of Hybrid Full Adder-22 Transistor

The above figure shows the simulation results of Hybrid Full Adder-22 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

The input signal A is given to inverter which consists of P1 and N1 transistors. Carry signal C_i is given to inverter which consists of P2 and N2 transistor[5]. The signal A is given to P3,P2 and signal B is given P2,N4.The output of P3,P2 are shorted together and is given to N4,the N4 is connected to N3.The signal A is given to N3 and signal B is given to N2.The

output of P3,P2 is given to inverter which consists of P4 and N5.The output of inverter is given to N6,N7,N8,P7.

The signal C_i is given to N6,P5,N7,P6,N9,P7.The input of inverter is given P6 ,P5,N9andP8.The output of transistors N6,P5 and N7,P6 are shorted together .The output is sum. The output of N8, N7 and N9, P8are shorted together and the output is carry. The circuit is simulated in 65nm technology and result are obtained.

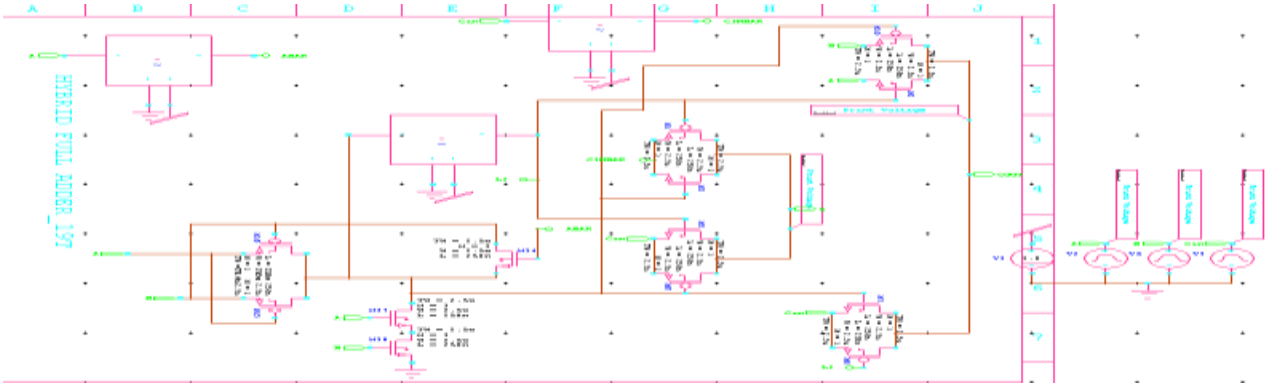


FIG 2.10: Simulation of Hybrid Full Adder HFA- 19T

The above figure shows the schematic of hybrid full adder - 19 transistors which is combinations of number of PMOS and NMOS logic is designed in 65nm technology .It is designed with tanner S-EDIT Tool.

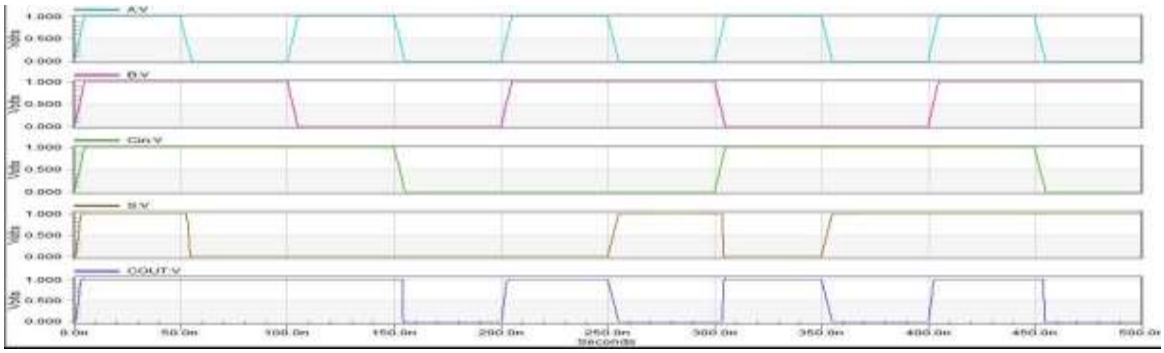


FIG 2.11: Simulation of Hybrid Full Adder-19 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner-SPICE[6] (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

III.PROPOSED METHOD

For computational arithmetic, a full adder is the primary logic units in VLSI applications. A new full adder circuit design has been presented in this article which is based on input switching activity pattern and gate diffusion input (GDI) technique.[7] The adder has been designed in two stages. The first stage is an XOR–XNOR module, whereas, the final stage is for the required outputs. By using the switching activity pattern of inputs and GDI techniques at each stage, the switching activities of the transistors have been minimized. This improves delay, power consumption and computational complexity. The adder has been designed and evaluated by using the synopsis tool and compared with different existing adder cells found in the literature. It is found that the presented adder shows an improvement at least 72.86% and 66.67% in terms of speed and energy consumption, respectively. Extensive performance analyses of the full adder have also been evaluated at 16 nm technology node which shows promising performances in both the technology nodes.

Summarily, the main contributions of the proposed work are listed below:

1. A 1-bit full adder circuit has been designed for VLSI applications based on switching activity and GDI technique which is compatible both with CMOS and CNFET technology.
2. The circuit has been designed in two stages. In the first stage, an XOR–XNOR [8]module has been designed, whereas, in the second stage the sum and carry modules have been designed. The overall circuit requires only 10 transistors.
3. By utilizing the switching activity pattern of the inputs and GDI techniques at each stage, the switching activities of the transistor (transitions) have been minimized during data flow from inputs to the outputs which ensures less delay and low power consumption.
4. Moreover, as C_{in} is introduced at the final stage, the initial circuit operation becomes independent of C_{in} that helps in further reduction in delay.

5. The simulations and analysis have been carried out in 90 nm CMOS, 32 nm CMOS and 32 nm technology nodes.
6. A comparative analysis has been carried out comprehensively to establish the utility of the proposed design.

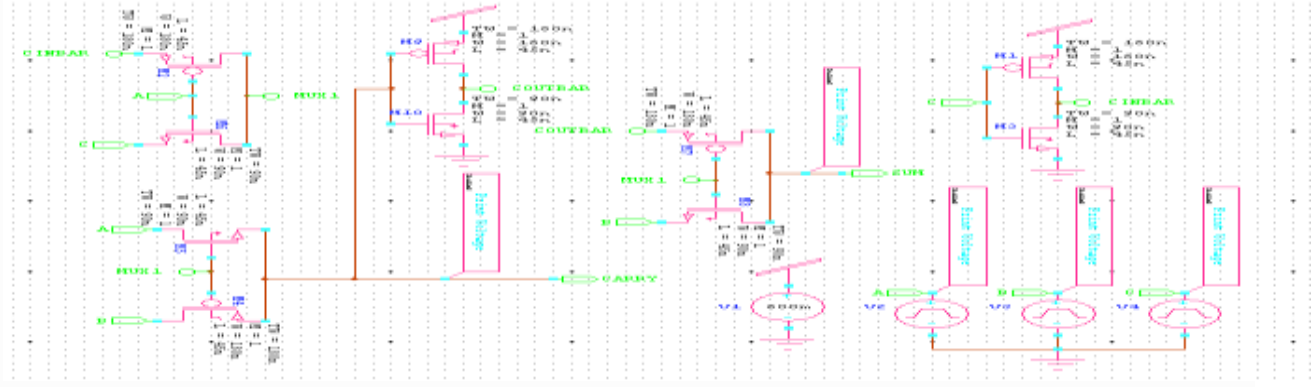


FIG 3.1: Simulation of Hybrid Full Adder-10 Transistor

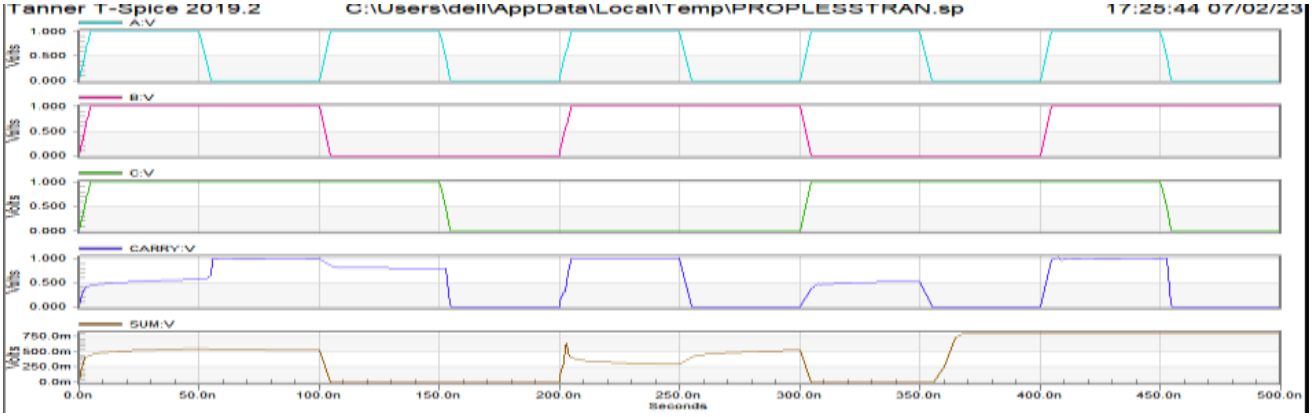


FIG 3.2: Simulation of Hybrid Full Adder-10 Transistor

The above figure shows the simulation results of Hybrid Full Adder-17 Transistor. It is simulated using CMOS Tanner-SPICE (Simulation Program with Integrated Circuit Emphasis) Tool. Wave forms are analyzed using W-EDIT(wave form editor).

IV.CONCLUSION

In this project first we evaluated XOR-XNOR schematics .The simulation shows that the NOT gates in circuit is disadvantage and another disadvantage is positive feedback. Due to this presence of feedback the delay,

output capacitance and power consumption are increased[9] .Then we propose new XOR-XNOR schematics that may not have the above listed disadvantages. By using proposed XOR-XNOR gates, we designed three new FA circuits for various algorithms. After simulation of FA circuits in various conditions, the results show that the proposed schematics has a very good performance in all simulation .simulation results show that the proposed FA schematics save PDP up to 23% comparison with other FA[10] circuit designs. The proposed FA designs have best speed and power.

V.FUTURE SCOPE

The need for low power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications. Increasing chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. Low power design is also required to reduce the power in high-end systems with huge integration density and thus improve the speed of operation.

REFERENCES

[1] N. S. Kim et al., “Leakage current: Moore’s law meets static power,” Computer, vol. 36, no. 12, pp. 68–75, Dec. 2003.
[2] N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th ed. Boston, MA, USA: Addison-Wesley, 2010.
[3] S. Goel, A. Kumar, and M. Bayoumi, “Design of robust, energy-efficient full adders for deep-submicrometer design using hybrid-CMOS logic style,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 12, pp. 1309–1321, Dec. 2006.
[4] H. T. Bui, Y. Wang, and Y. Jiang, “Design and analysis of low-power 10-transistor full adders using novel XOR-XNOR gates,” IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, pp. 25–30, Jan. 2002.
[5] S. Timarchi and K. Navi, “Arithmetic circuits of redundant SUT-RNS,” IEEE Trans. Instrum. Meas., vol. 58, no. 9, pp. 2959–2968, Sep. 2009.
[6] J. M. Rabaey, A. P. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, vol. 2. Englewood Cliffs, NJ, USA: Prentice-Hall, 2002.

[7] D. Radhakrishnan, “Low-voltage low-power CMOS full adder,” IEE Proc.-Circuits, Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[8] K. Yano, A. Shimizu, T. Nishida, M. Saito, and K. Shimohigashi, “A 3.8-ns CMOS 16×16-b multiplier using complementary pass-transistor logic,” IEEE J. Solid-State Circuits, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[9] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, “Performance analysis of low-power 1-bit CMOS full adder cells,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, pp. 20–29, Feb. 2002.

[10] N. Zhuang and H. Wu, “A new design of the CMOS full adder,” IEEE J. Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992