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An Efficient 2x2 And 4x4 SRAM Array By Using Compact Decoder For Low Power & Low Area Applications

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Abstract

SRAM act us cache memory such as L2 and L3 in CPU and also used as interface between the CPU and DRAM. SRAM provides high operating speed and low power consumption due to not refreshing the memory content every time. It used transistor to store the data. But the cost is high and low memory capacity and low storage capacity. In order to reduce the cost, the compact (i.e.) less number of transistors based SRAM array play vital role in cost effective memory design. The main aim of this work is to design a compact SRAM memory array for low power, low area and low cost applications. Power optimization is performed by using various ways such as logical minimization using K-map, truth table reduction and Shannon's theorem. In this work, truth table reduction scheme is used to design a compact AND gate of decoder for SRAM array. Also the compact 1 to 2 decoder and 2 to 4 decoder are used in 2x2 SRAM array and 4x4 SRAM array by using 6T SRAM cell. Also CMOS 22nm nanotechnology is used for transistor scaling scheme. From the analysis, the 6T SRAM cell based 2x2 and 4x4 SRAM array with compact decoder offers low cost, low resource utilization and low power consumption than the regular decoder based SRAM array.

Keywords: Truth Table Reduction, Decoder, SRAM cell, 2x2 SRAM array, 4x4 SRAM array, Low power and Low cost

1. Introduction

In these days scientific alters, there is a drive to extend the devices for example memory with a high Speed and low power. They have revolved into a insightful piece of several VLSI ICs. A memory unit is a corporeal device which is utilized to store agendas or information on an enduring or impermanent basis for utilize in digital electronic scheme's. Static-Random-Access-Memory (SRAM) is a static memory cell extensively utilized in different electronic schemes, considerably in elements employed for cache memory in microchips, memory, engineering workstations, and mainframe computers in hand-held apparatus owing to low power consumption and high speed. SRAM is a kind of semiconductor memory by means of bi-stable latching circuit to hoard every bit and displays data reminisce that is remaining of information constant after reiterated removal efforts, however is still volatile specifically information is lost when the memory is not power-driven. A universal SRAM array consists of the chief SRAM construction blocks are - row decoder, write driver circuit, pre-charge circuit, SRAM cell and sense amplifier circuit.

The SRAM with low power have become a critical module of several VLSI ICs. This is particularly right for microprocessors; anywhere the on-IC cache dimensions are raising with every generation to viaduct the rising deviation in the velocity of the main memory and the processor [P. Barnes2010, S. Hesley, et.al, 2009]. Owing to the raised incorporation and in service power dissipation, speeds has become a significant deliberation together in addition to because of the volatile enlargement of battery functioned appliances. There are two reasons of an SRAM design: primary is to give a straight interfacing with CPU at quickness not achievable by DRAMs and next is to substitute DRAMs in schemes that the need extremely low-power use.

In the main roles, the SRAM works as cache-memory and also interface between the CPU and DRAMs. The next driving force for SRAM scheme is low power appliances. In this case, S RAM are utilized in mainly moveable tools for the reason that the DRAM revive current is more than a few orders of scale in excess of the low-power SRAM stand-in current. They initiated to construct SRAM with two aims, primary to lower the operational voltage starting 3V to 1.8V. Next to diminish static and active power use for battery operated appliance. Other than it has been examined that the immovability of memory is gravely affected by reduce in supply voltage (VDD) [Evelyn Grossar 2006].

Scaling of scheme will collision on many factors for example, channel length, gate oxide thickness and the supply voltage should

be decreased. In upcoming, the Gate Oxide thickness perhaps as Low as 0.15nm on behalf of CMOS scheme. As a outcome the diminution in gate oxide thickness raises sub threshold leakages and gate leakage current in CMOS circuits. These will outcomes negative gate voltage and high drain voltage, field crowding arises at drain edge causing GIDL (gate induced drain leakage). In addition this high drain voltage appliance to a short channel machine outcomes in decreasing of barrier height and changing of point of utmost barrier to the left causing DIBL (drain induced barrier lowering). If the supply voltage is lower the threshold voltage, the procedure parameters and the unpredictability of the SRAM raise harshly. A few of the SRAM stability problems are threshold voltage random variation, diminishing ION / IOFF and procedure-provoked device deviation. Because of raise in Vt oscillations and process deviations, SRAM cell cannot be functioned at additional scaled supply electrical energies without serviceable breakdowns producing yield loss.

SRAM cell is a one of the high-speed memory cell which is used for high speed functions like caches and buffers. The cause SRAM is utilized in this appliance is that it is quicker than DRAM which is as well employed as a memory cell other than it is constituted of capacitors whereas the additional hand SRAM is constructed by using transistors. Thankfulness to technical innovations we can now integrate millions of transistors on a solitary chip. At the same time as this allowed us to attain operations with diminished size, it is as well significant that their recital should be leveled as said by the present requires. It seems like you're discussing some technical aspects related to memory cells and their performance. If you have a specific question or topic you'd like to explore further, feel free to ask. It looks like you're talking about the trade-offs involved in scaling memory cells, where reducing their size can lead to increased power consumption due to seepage current, ultimately impacting the overall performance of the memory cell. Power consumption, cost, and speed are all important factors to consider in designing and optimizing memory systems. If you need more information or have a specific question, please provide additional context. To prevail over this, they utilize a self-voltage level (SVL) circuit in connection with SRAM cells. In that work they, will be seeming at forming an 8x8 memory cell array contains 7T SRAM cells with the mixture of SVL circuit with CMOS transistors at 28nm to conquer the extra power consumption owing to the leakage current. Every part of the schema executions are carried out on cadence virtuoso at 28nm schemes. In this work, further to improve the dynamic power of the SRAM array, the truth table reduction scheme is used to construct a novel decoder circuit.

After this decoder are incorporated into the 2x2 and 4x4 SRAM array for low power consumption, low cost and low die size.

2. Literature Survey

The chief intention of this work is to construct 16*16, 8*8, and 4*4 SRAM array using 7T and 6T SRAM cells based on Graphene Nano Ribbon Field Effect Transistor (GNRFET) scheme and contrast power dissipation between GNRFET and CMOS schemes. The GNRFET complexity is high, performance is low because of edge roughness effect but provide low power dissipation than the CMOS [1]. In this work an attempt is completed to construct and imitate a Low power 16×16 SRAM Memory Array using 7T I-LSVL SRAM Cell. Secondary components of whole 16×16 SRAM Array like Row decoder, Column decoder, Sense amplifier are constructed. The Power utilization of suggested 16×16 SRAM Memory Array is 18.3mW which is an enhancement of 8.66% [2].

Design of ternary 2X2 SRAM memories Array-based on carbon Nano-tube field-effect transistor's (CNTFETs) is presented which find the recitals such as power consumption, area, speed and current driving capability of circuits have been analyzed. From the analysis, the complexity is high. But the power is low [3]. The 8T SRAM cell based 4x4 SRAM array is designed by using tanner tool 13.1. The functionality of this SRAM array is verified but power and area calculation are not done [4]. In this work, the Adaptive-Voltage-Level (AVL) circuit is incorporated into Asymmetric 10T-SRAM cell, to shrink the sub-threshold leakage and in addition to gate leakage, which manages the effectual voltage across the SRAM cell in inactive form [5]. Also Simulations are carried out with 90nm CMOS technology. The conventional 6T based 4x4 SRAM array and suggested 10T based with AVL 4x4 SRAM requires high power consumption compared to proposed 4x4 SRAM array. In this work 6T SRAM cell are designed by using 250nm and 180nm CMOS technology. Hence the power consumption is very high [6]. The 8T and 6T based back gate biasing SRAM array based on row and column-based selection are designed and area are calculated. It does not calculate the power value [7].

In this work, 2x2 SRAM array using 6T is designed by using reversible logic gate. The power consumption is very low compared to non-reversible logic based 2x2 SRAM array. But compared to our proposed technique, this power consumption is very high [8]. Analysis of different SRAM cell such as 6T, 7T, 8T and 9T are performed and concluded that the 9T based SRAM is best for low power consumption. Also 120nm CMOS technology is

used. It does not include recent Nano technology [9]. In this work, self-controllable Voltage Level (SVL) is used to construct proposed 7T SRAM cell. Then it will compare into regular 7T SRAM cell. Finally, it will used to construct 8x8 SRAM array. But the power of 8x8 SRAM array is not calculated [10].

In this work only one bit SRAM is designed. But not designing 2x2 and 4x4 SRAM array. It designed only 6T SRAM cell based 1bit SRAM [11]. 1KB SRAM array is designed by using 8T and 10T based SRAM cell. 32x32 SRAM array is formed and calculated corresponding power consumption and delay. Also 45nm only used. But we are using 22nm technology [12]. The 8T SRAM cell is designed using Advanced Sub threshold scheme. The area is high due to adding two extra transistors. But the speed is high [13]. Here only 32nm nanotechnology is used but we are using 22nm nanotechnology. Also FINFET based 4x4 SRAM array using 6T SRAM cell design complexity is high [14]. Binary and quaternary 4x4 SRAM array are designed and analyze the power consumption. The Quaternary D Latch based 4x4 memory array offers low power when compared to the binary 4x4 SRAM array. But they used only 180nm and 90nm. They are not used advanced nanotechnology [15].

ULP 8T SRAM cell is designed and 2x2 SRAM array is constructed, which is used for object detection and tracking purpose based on macro block resizing. Accuracy, complexity are calculated. The ULP based 8T SRAM offers low power consumption, high accuracy and high speed [16]. The 9T SRAM cell and 6T SRAM cell are designed and analyzed power and delay of these two SRAM cell. The 9T SRAM cell offers low power and low delay than the 6T SRAM cell. But compared to our proposed scheme, power consumption is very high [17]. Regular CMOS, Gated VDD and MTCMOS based SRAM cell designed with 130nm technology. From the analysis, the MTCMOS based 6T SRAM cell offers low power and low delay than the all other existing scheme [18]. CMOS, Mixed logic and GDI based 4x4 SRAM array and 16x16 SRAM array are designed by using line decoder. From the analysis, the GDI based line decoder and SRAM array offers low power, low area and low delay compared to conventional technique. But the numbers of transistors, power are very high compared to our technique [19].

3. METHODOLOGY

3.1 Design of 6T SRAM cell

The demands for low power of the SRAM units have compelled several investigators in the direction of novel low-power circuits.

Six transistors have been extensively identified as an appropriate option for low-power appliances. Figure. 1 illustrates a standard 6 transistor SRAM cell which embraces one bit of information in an SRAM cell.

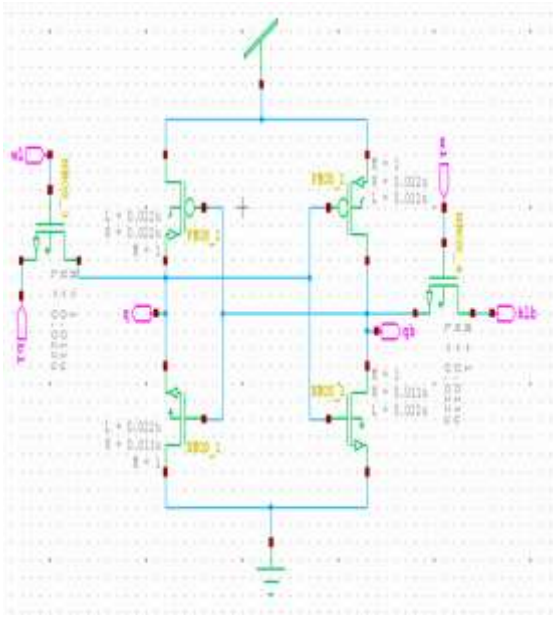


Fig.1 Circuit diagram of 6T SRAM cell

It usually contains two access transistors and a loop of two inverters. The NMOS transistors NMOS_2 and NMOS_1 are also known as drive transistors and are answerable for releasing the bit line for the duration of the read process. Transistors NMOS_3 and NMOS_4 are called access transistors. Once on it permit the interior nodes of the cell (i.e., node B and A) to converse with the bit lines. The access transistors which have the gate terminal also referred to word line (WL). The PMOS transistor's of PMOS_1 and PMOS_2 known as the load transistor's. Based on the logic value presented in the cell, one of the inner nodes of the unit is at VDD and the additional one is at VSS. The cell leakage current when it is non-accessed is exposed in the depiction. The seepage current is first and foremost because of the sub-threshold current and next because of Gate-Induced-Drain-Leakage (GIDL). In the following sections it will be exposed that the leakage current has the opposite exponential affiliation with the threshold-Voltage of the transistor's. The six transistor's based SRAM cell is designed to construct 2x2 and 4x4 SRAM array.

Access transistors provide for read and write access to the cell. An SRAM cell provides the pursuing fundamental properties:

Retention: An SRAM cell is capable to hold the information for an indefinite period on condition that it is powered.

Read: An SRAM cell is capable to converse its information. This procedure does not affect the information specifically Read process is non-destructive.
Write: The information of an SRAM cell can be put to any double value in spite of its unique data.

3.2 Design of a novel 1:2 and 2:4 compact decoder

A row decoder and a column decoder are used to trigger the particular word line and bit line as said by the address. The circuit diagram of 1:2 decoder is shown in fig.2. It contains one inverter and 2 AND gate. Decoders are utilized at what time we require to input data to a particular output line. The core memory of computer is addressed by using decoder in that we have an individual memory location to store the input information.

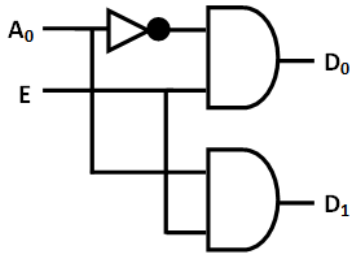


Fig.2 Circuit diagram of 1:2 decoder

If the number of transistors in AND gate reduced, the number transistor in decoder are reduced. Hence the truth table of AND gate shown in table.1 is simplified into table.2 based on truth table reduction scheme. The reduced AND gate truth table is used to design a compact AND gate circuit.

Table 1 Truth table of AND gate

A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

Table 2 Reduction table of AND gate

A	B	Y=A.B
0	X	0
1	X	B

The AND gate truth table are reduced by using don't care condition. When input A is 0 B is 0 or 1, the corresponding output is zero. Conversely, when the input A is 1 and B is zero or one, the output is B i.e. B 0 means output 0 and B 1 means output 1. This reduced truth table is used to design a novel AND gate circuit as shown in fig.3.

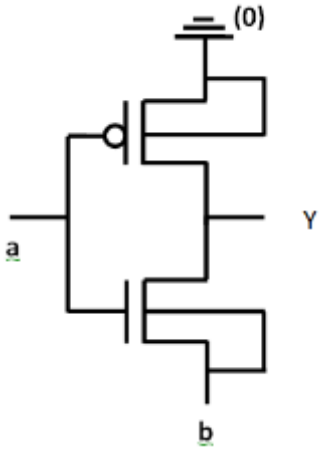


Fig.3 Circuit diagram of a novel AND gate

When A=0, B=0 means, the PMOS in on NMOS is off. PMOS is connected to ground. So the output is zero. Next the input A=0, B=0 means, PMOS only on but it will connected to ground. Hence the output is zero. During A=1, B=0 means, NMOS on and PMOS off. NMOS is connected to B, the corresponding B value 0 as output. Finally A=1, B=1 means, only NMOS on. This NMOS is given into B. So the B value 1 given as output for this condition.

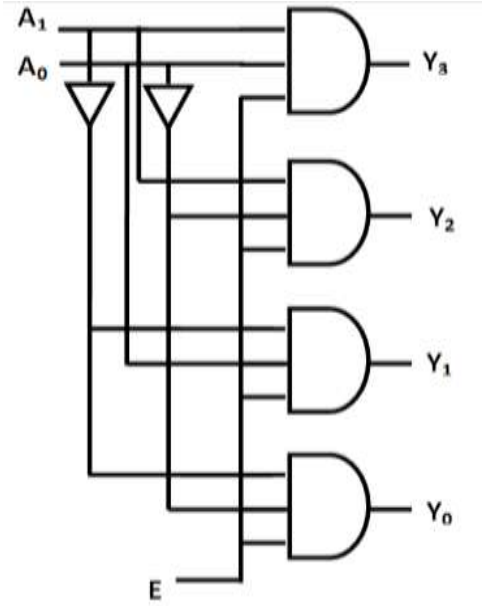


Fig.4 Circuit diagram of a 2 to 4 decoder

The 3 input AND gate is designed by using 2 two input AND gate. The 2 to 4 decoder needs two inverter and 4 three input AND gate (i.e.) 8 two input AND gate. In the conventional 2 to 4 decoder is designed by using static CMOS technology. AND gate using static CMOS logic require 6 transistors. But the proposed AND gate needs only 2 transistors as shown in fig.3. Hence 8 two input AND gate require only 16 transistors for proposed 2 to 4 decoder. But the conventional 8 two input AND gate requires 48 transistors instead of 16 transistors. Similarly the proposed 1 to decoder needs 6 transistors (2transistors inverter+ two 2 transistors AND gate). But the existing static CMOS based decoder needs 14 transistors (2transistors inverter+ two 6 transistors AND gate). Hence the proposed 1 to 2 decoder and 2 to 4 decoder offers low area and low power consumption than the conventional 1 to 2 decoder and 2 to 4 decoder.

3.3 The 2x2 and 4x4 SRAM array design

The 2x2 SRAM consists of 1 to 2 row decoder, 1 to 2 column decoder, write driver, Precharge circuit, 4 SRAM cell (2x2) and sense amplifier circuits. Row and column decoder are used to select particular data selection in the memory location. The Precharge circuit contains 3 PMOS. It used for charging purpose. Write driver is used to write the data in the memory during the write enable signal is high. The voltage latch sense amplifier is used to achieve low power consumption instead of current latch sense amplifier. Finally the output is drive when the SE is zero.

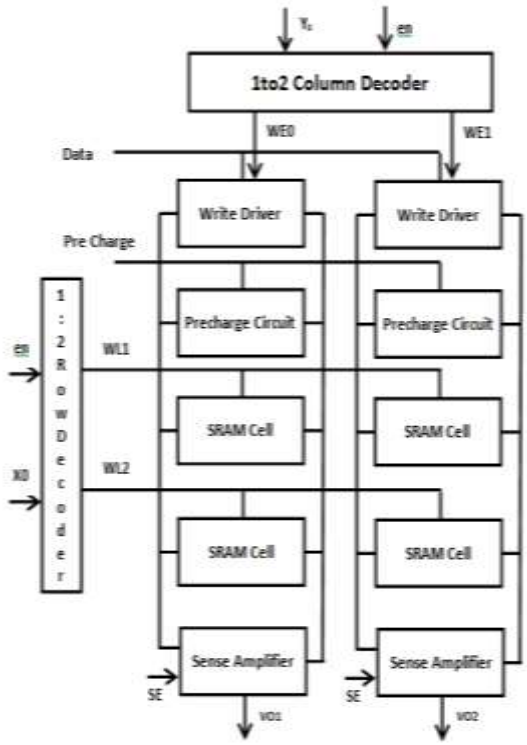


Fig.5 Block diagram of 2x2 SRAM array

Similarly the 4x4 SRAM array is designed by using 16 SRAM cell. Also compact 2 to 4 decoder row decoder and column decoder are used to achieve low die size and low power consumption. The block diagram of 4x4 SRAM array is shown in fig.6. The write enable signal is generated from column decoder. Conversely write line signal is produced by row decoder. The data is given into write driver circuit. The Precharge signal is given to precharge circuit for charging. Finally, the conventional 2x2 and proposed 2x2 SRAM array are constructed to analyze area and power utilization. Likewise, the existing 4x4 and proposed compact 4x4 SRAM array are designed to examine the number of transistors required and total power consumption.

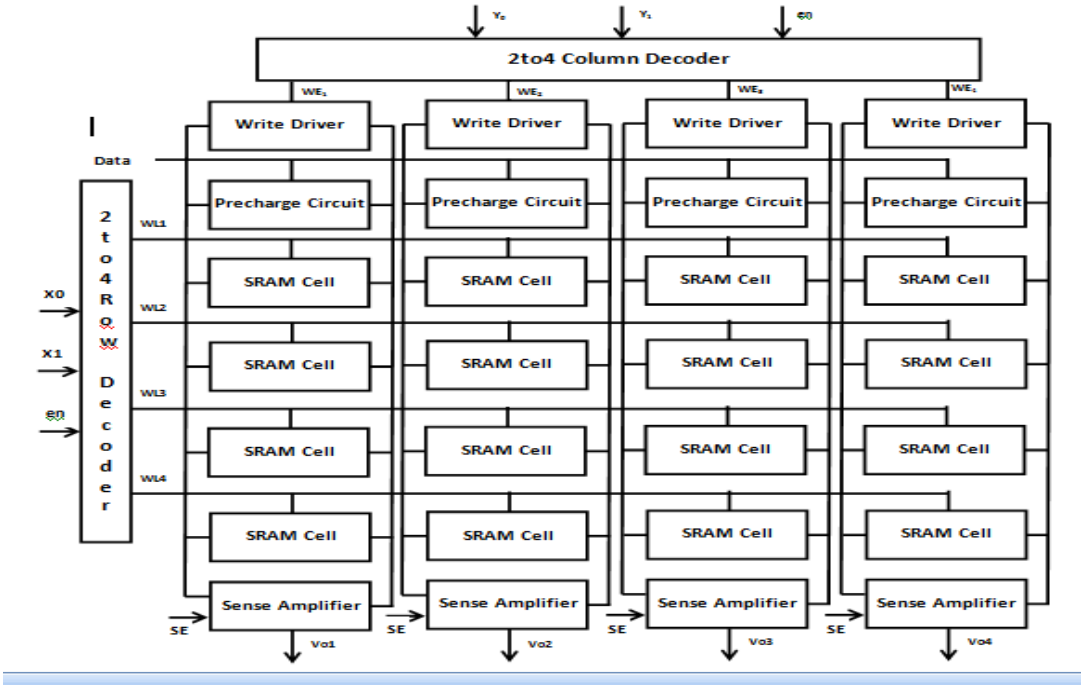


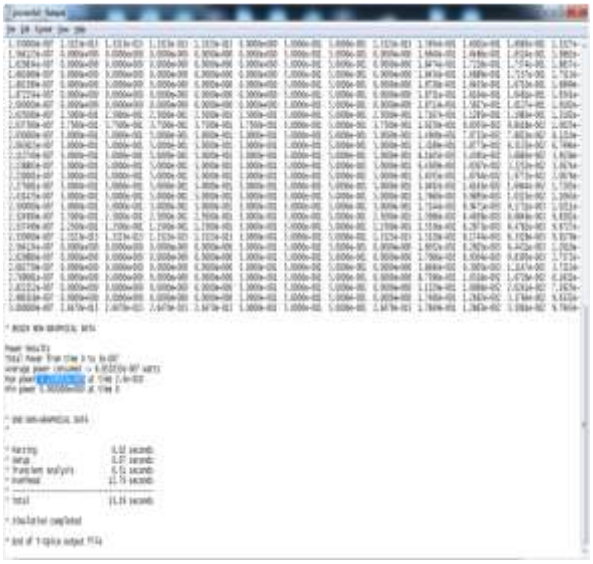
Fig.6 Block diagram of 4x4 SRAM array

4. RESULTS AND DISCUSSION

Initially different types of SRAM cell are designed to analyze the number of transistors required and total power consumption by using tanner tool 14.1. After that four types of decoder are designed to construct 2x2 and 4x4 SRAM array. The comparison between conventional and proposed decoder are performed to identify which decoder is best for low power application. Finally, the compact 1:2 decoder and compact 2:4 decoder are used in proposed 2x2 SRAM array and 4x4 SRAM array.

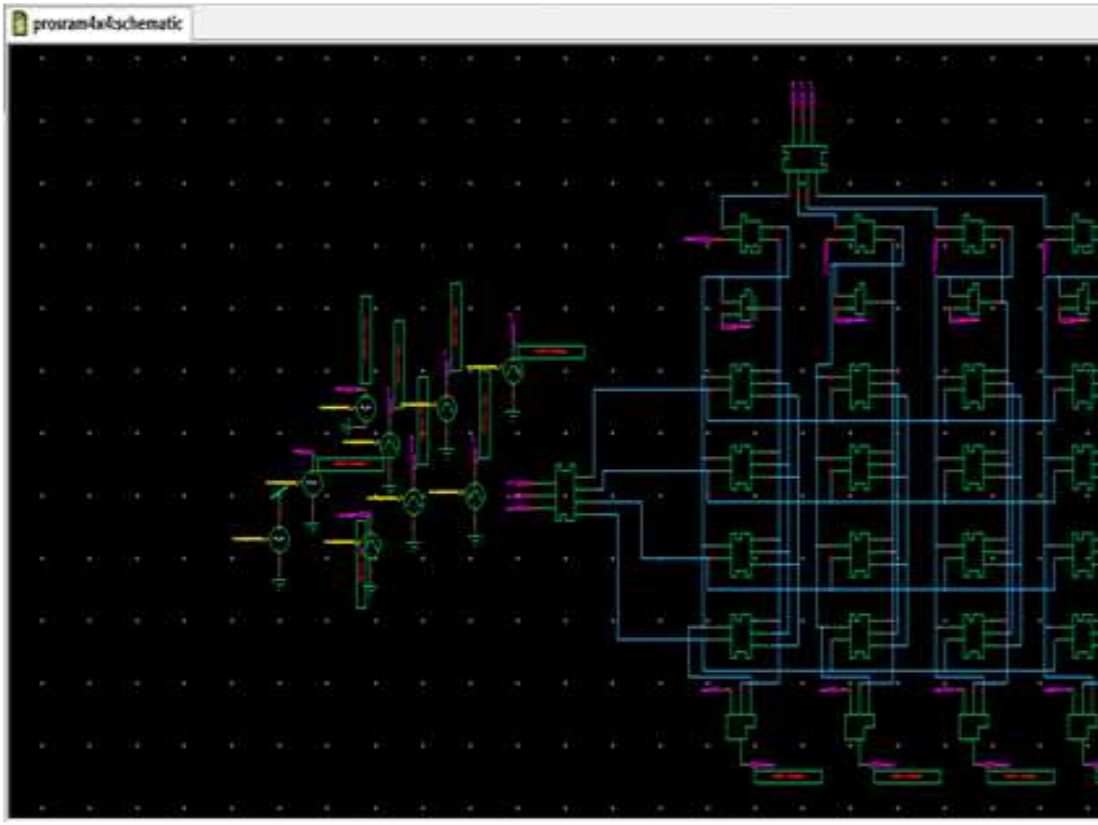
Table 3 Comparison of different types of SRAM cell

Types	No of transistors (Area)	Power (uw)
SRAM-6T	6	0.755uw
SRAM-6T[6]	6	3.146mw
SRAM-7T[10]	7	0.771uw
SRAM-9T [17]	9	802uw (0.802mw)
SRAM-6T [20]	6	0.935uw
SRAM-6T [21]	6	152.37uw



Power output of proposed 4x4 SRAM

Area output of proposed 4x4 SRAM



Schematic of proposed 4x4 SRAM

Fig.7 Design and Implementation result of 4x4 SRAM array

From the analysis of table.3, the proposed 6T SRAM offers low power than the all other state of arts technique. The proposed 6T SRAM cells offers 19.25% power reduction than the reference paper [20], 99.5 % power reduction than [21], 99.9% power reduction than [17] and 2% power reduction than reference [10].

Table 4 Comparison between existing and proposed 2x2 SRAM array

SRAM Array	No of transistors (Area)	Power (uw)
2x2 with regular 1:2 decoder and 6TSRAM cell	84	21.5uw
2x2 with compact 1:2 decoder and 6TSRAM cell	68	18.9uw
2x2 SRAM [8]	-	1.005mw or 1005 uw

The proposed 2x2 SRAM array provides 19.4% area reduction and 12.9% power reduction than the conventional 2x2 SRAM array. Similarly 98.61% power reduction than the reference paper [8].

Table 5 Comparison between conventional and proposed 4x4 SRAM array

SRAM Array	No of transistors (Area)	Power (uw)
4x4 with regular 2:4 decoder and 6TSRAM cell	264	66.41
4x4 with compact 2:4 decoder and 6TSRAM cell	200	52.19
4x4 SRAM [5]	-	304.466
4x4 SRAM [19]	2100	0.87mw or 870uw

The proposed 4x4 SRAM array with compact decoder offers 24% area reduction and 21% power reduction than regular decoder based 4x4 SRAM array. Also the proposed 4x4 SRAM array gives 90.47% area reduction and 94.11% power reduction than the reference paper [19].

5. CONCLUSION

Two types of decoder are designed such as regular 1:2 and 2:4 decoder and compact 1:2 and 2:4 decoder are designed for 2x2

and 4x4 SRAM array with compact 6T based SRAM cell. Also results are analyzed. From the results, the proposed 6T SRAM with 22nm offers low power consumption than the all other existing work. After that two types of 2x2 SRAM array are designed with regular and compact 1:2 decoder. The proposed compact decoder based 2x2 SRAM array is best for low area and low power applications compared to regular decoder based 2x2 SRAM array. Conversely, the proposed 4x4 SRAM array with compact 2:4 decoder used for low die size and low power portable cache memory applications when compared to the regular 2:4 decoder based 4x4 SRAM array. The proposed 2x2 SRAM array offers 32.3% APP (area power product) reduction than the regular 2x2 SRAM array. Also the suggested 4x4 SRAM array provides 45% APP reduction than the conventional 4x4 SRAM array. In future, large size SRAM array will be designed such as 16x16, 32x32… etc for large bit size SRAM memory applications.

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